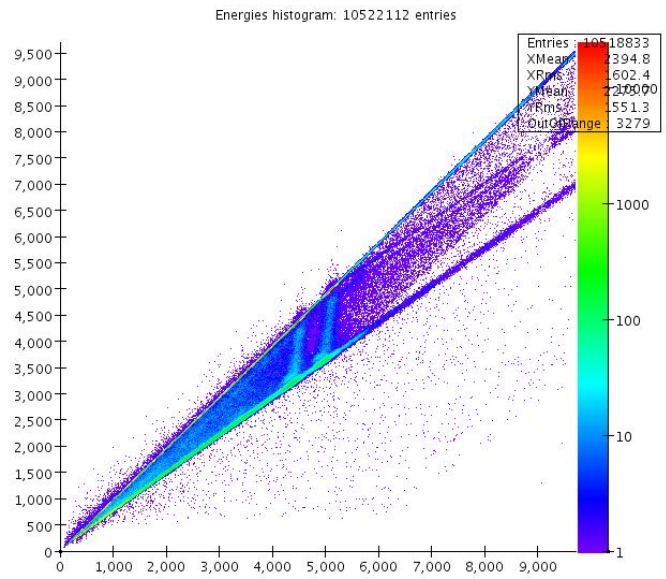
Electronic development for Phoswich at IPHC

Summary

- Energy measurement @ 100 MHz with TNT2 Card
- Software development
- Trigger development for Pile up rejection
- Timing measurement
- Voltage divider
- Preamplifier Card

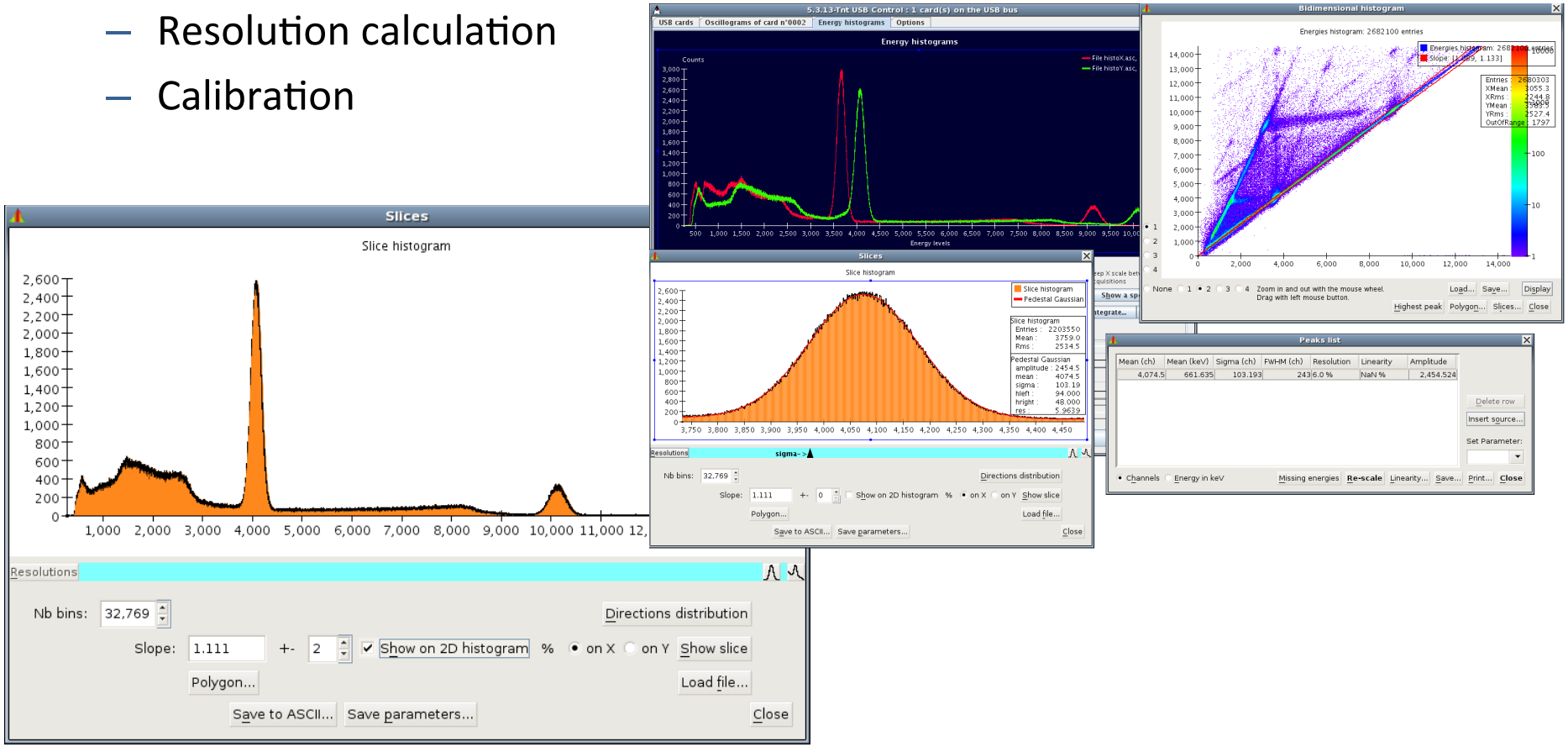
Measurement with TNT2 Card

- Test Setup at Orsay
  - PW coupled with a Hamamatsu R7723-100 PMT
  - Cremat CR-113 Préamplifier;
    - decay time 50 μs (Cf=750pF, Rf=68kΩ)
  - 2 channels of modified TNT2 Card
    - 14 bits, **100 MHz**
    - Dynamic range 24 MeV
    - Counting rate 8 to 20 kHz
- Results
  - @ 662 keV
    - **4.7%** in LaBr3
    - **7.2%** in NaI
  - **Same result than with 1 GhZ Digitizer**



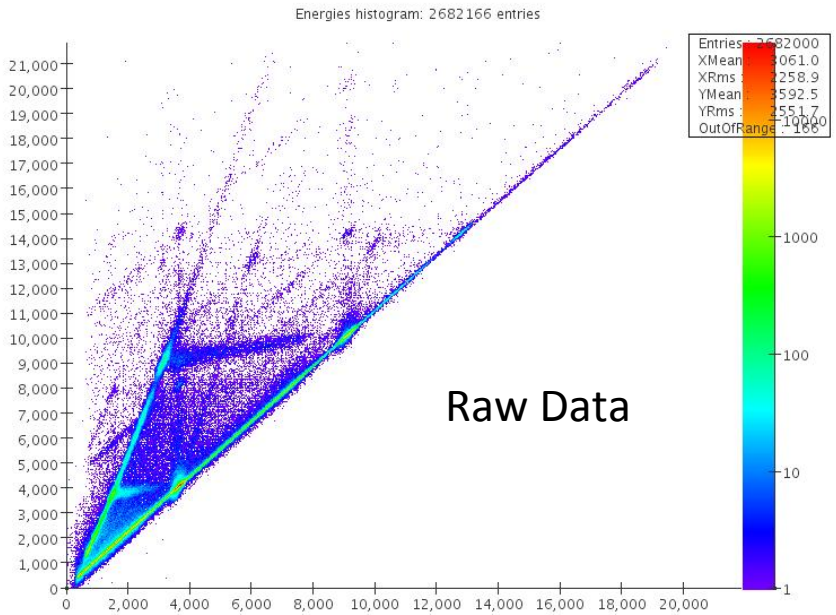
TNT2 interface development

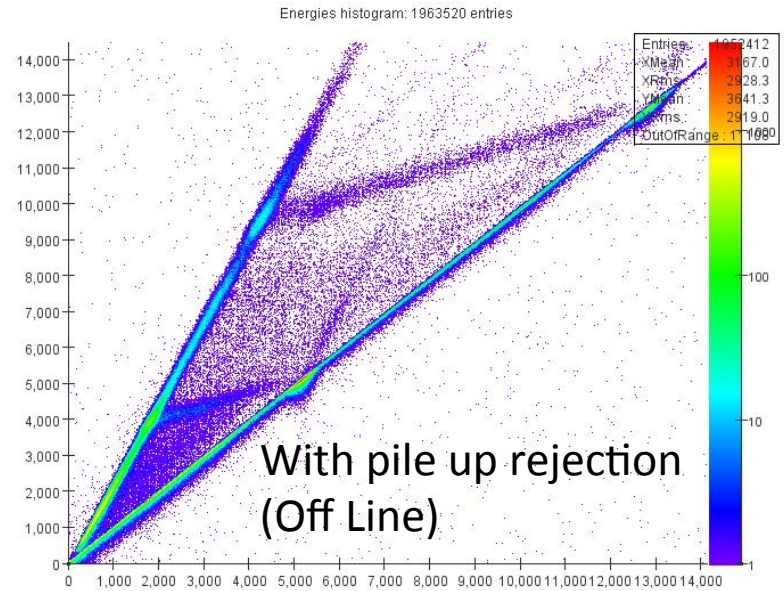
- On line tools in TUC acquisition system
  - Bi-dimensional spectra
  - Graphical selection / Projection
  - Resolution calculation
  - Calibration



Pile up rejection

- Trigger algorithm development



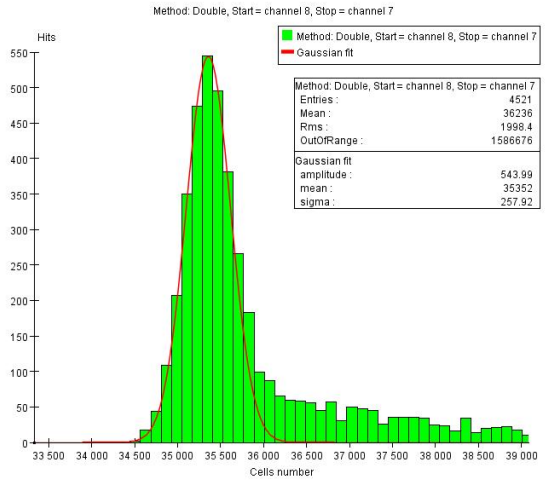


- To be implemented in TNT2 Card soon

Preliminary result for Timing

- Experimental Set Up 1
  - Timing measurement between LaBr3 signal from PW and a small (1”*1”) pure LaBr3
  - Anode send in external CFD and digitalized at 250 MHz (DT5 Card)
  - Timing measured in a digital TDC (implemented in FPGA) develop for DT5 card

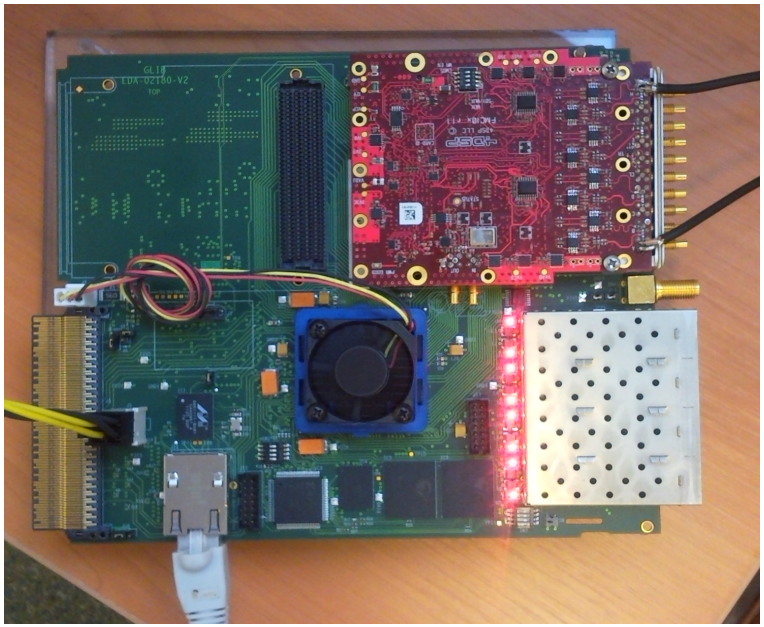
- Result: **Sigma=250 ps** for ^{60}Co



- We already test a full digital solution at 100 MHz digitalization and the algorithm developed by Bardelli et al. (NIM A, 521, 480-492 (2004)); Sigma= 900 ps

GLIB : Gigabit Link Interface Board (CERN)

- To be tested for timing (GANAS)



- Advanced Mezzanine Card module for µTCA environment or bench-top use.
- Based on a Virtex-6 FPGA with 6.5Gbps transceivers.
- Four pluggable 10Gbps optical transceiver modules (SFP+).
- Two expansion FPGA Mezzanine Cards (FMC108) and up to four additional 6.5Gbps transceiver lines (optional).

FPGA Mezzanine Card: FMC108

- □ 8-Channel ADC 250MSPS @ 14-bit
- □ External reference clock
- □ External Trigger
- □ LVDS or 1.8V LVCMOS output operation
- □ HPC (High-Pin Count) 400-Pin Connector

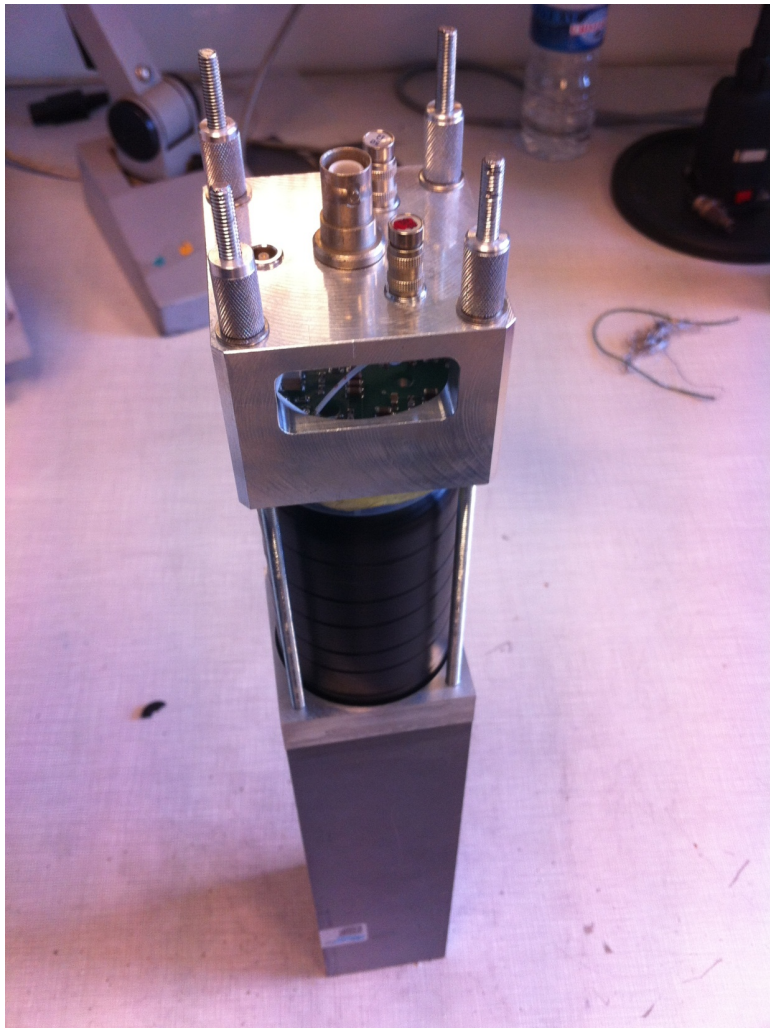
- Compatible with GTS (Virtex6)
- 10 k€ for 16 channels

Voltage Divider development

- Mechanically compatible with Cluster
- Tapered configuration of the voltage divider proposed by Hamamatsu

Electrodes	K	Dy1	Dy2	Dy3	Dy4	Dy5	Dy6	Dy7	Dy8	P
Standard ratio	4	1	2	1	1	1	1	2	1	
Tapered ratio	6	1	2	1	1.2	1.5	2	4.5	2	

- Around 100€ / PMT (with 3 output)



Preamplifier Card development

- 5 Channel (Phoswich)
- Compatible with Cremat CR11X preamplifier
- For each channel
  - 1 Input Lemo (1 MΩ)
  - 1 input for test
  - 2 Output Lemo (50 Ω)
  - 1 Output sma
  - 1 Attenuator
    - 7 gain from 0 to 20 db
  - 1 offset correction

- 270 €/channel for 3 NIM card (15 channels)

To conclude

- We could build some more Voltage Divider and preamplifier Card if needed

- preamplifier Card + TNT2 Card coupled with the TUC acquisition system could be a good solution to test one (or two) cluster