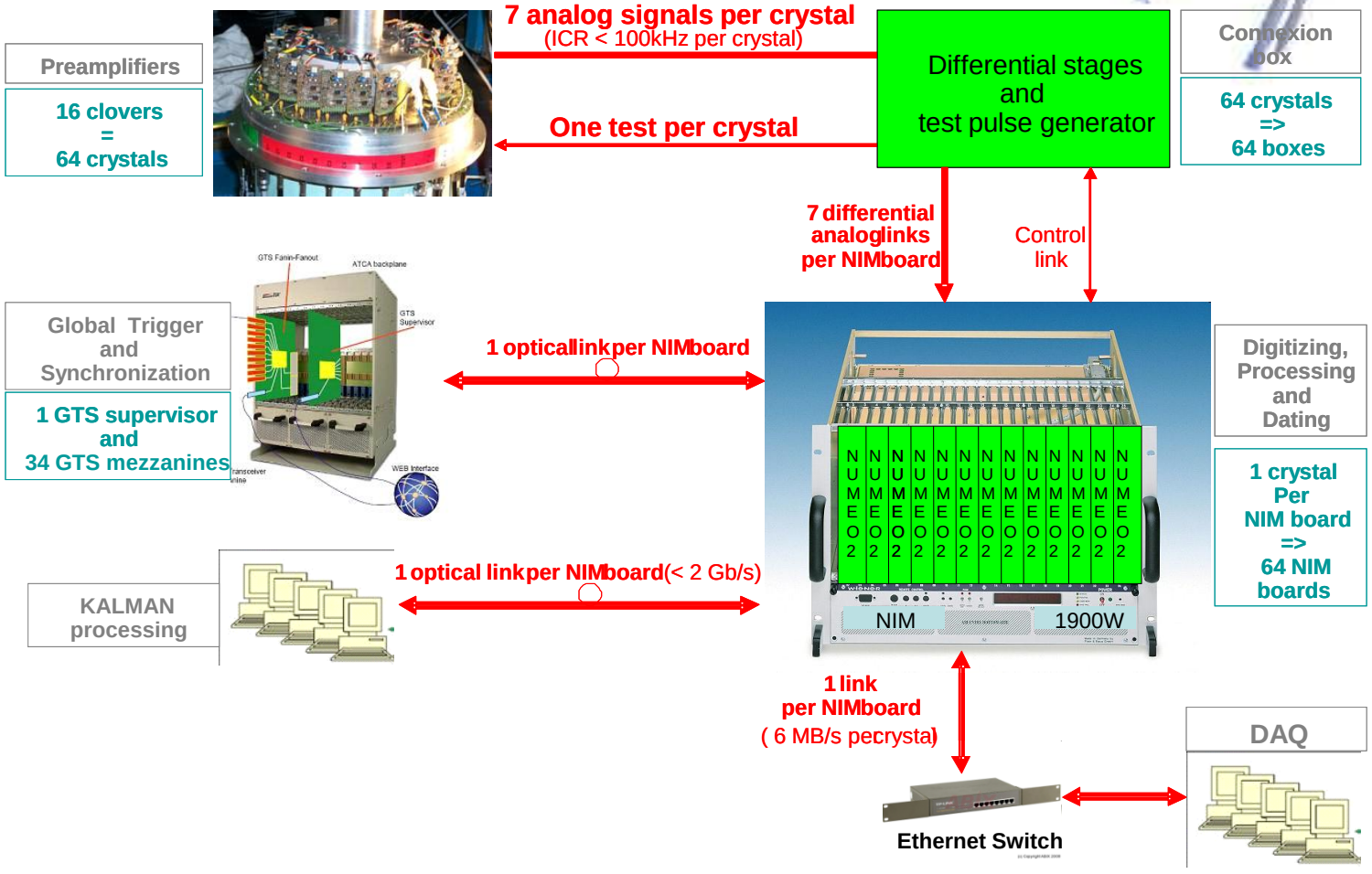
EXOGAM2 Status Report

G de France, GANIL

PARIS Workshop, Bormio, February 21, 2012

General layout



Connection box (GANIL)

Role:

- Common => differential mode for 1 Xtal (7 signals)
- Test generator.

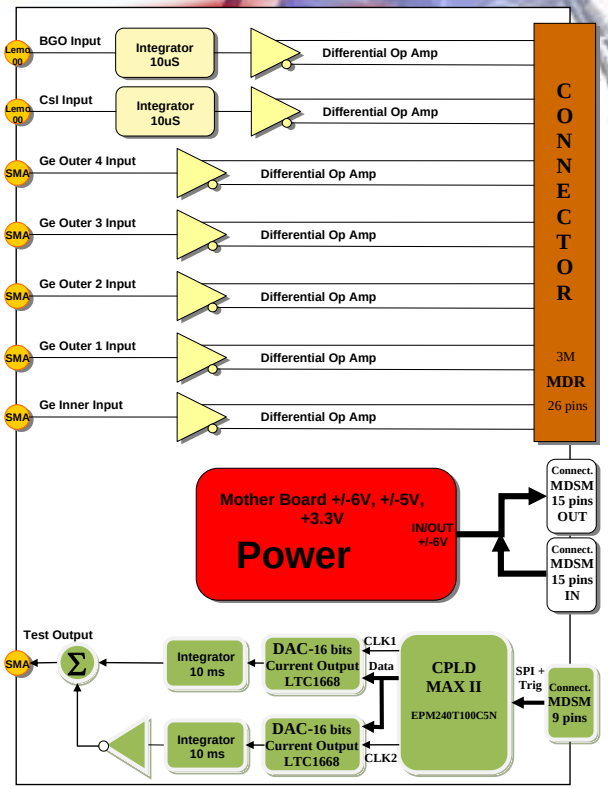
Specs:

16 clovers ➔ 64 connection boxes

- Detector channels:
  - -Analog inputs: 1 Ge inner, 4 Ge outer, 1 BGO, 1 CsI
  - -Analog outputs: differential 100Ω
  - -Gain: G=1 for Ge ; 3<G<15 for BGO and CsI (potentiometer)
- Test generator:
  - -Pulse output: 0 to 1V on 50Ω; polarity and amplitude are software controlled
  - -Tail pulse: 10ms
- Rate and trigger: software or NIM trigger input controlled

Status:

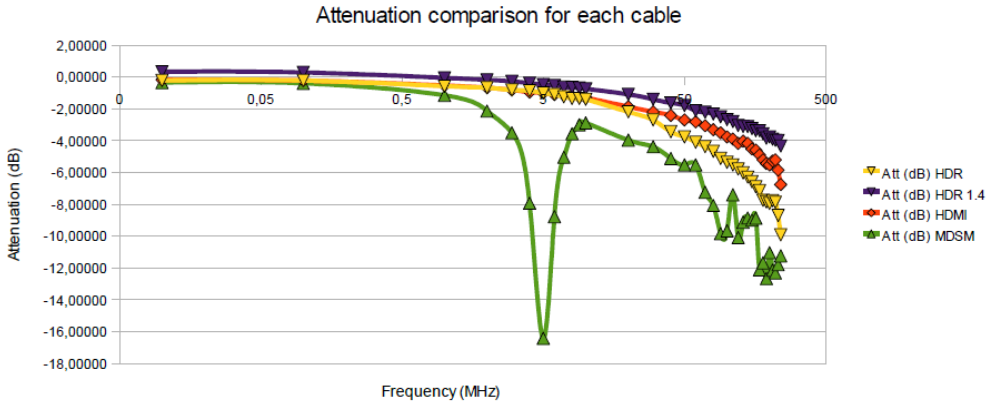
- Prototype under test



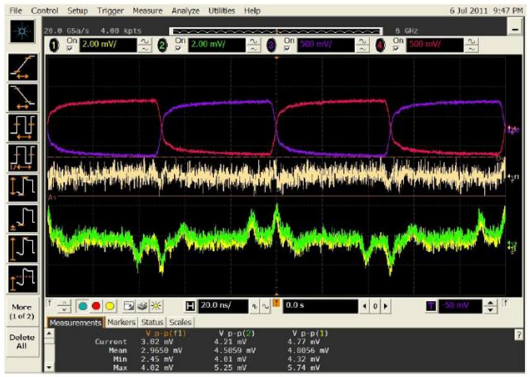
Cables: connection box to digitizer (GANIL, Valencia)

Status:

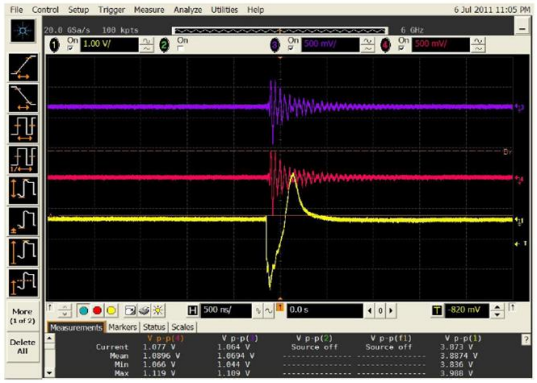
- Various cables tested
- HDMI cable chosen



HDMI cable: ts=tf=2.5 ns



EMC results for HDMI cable

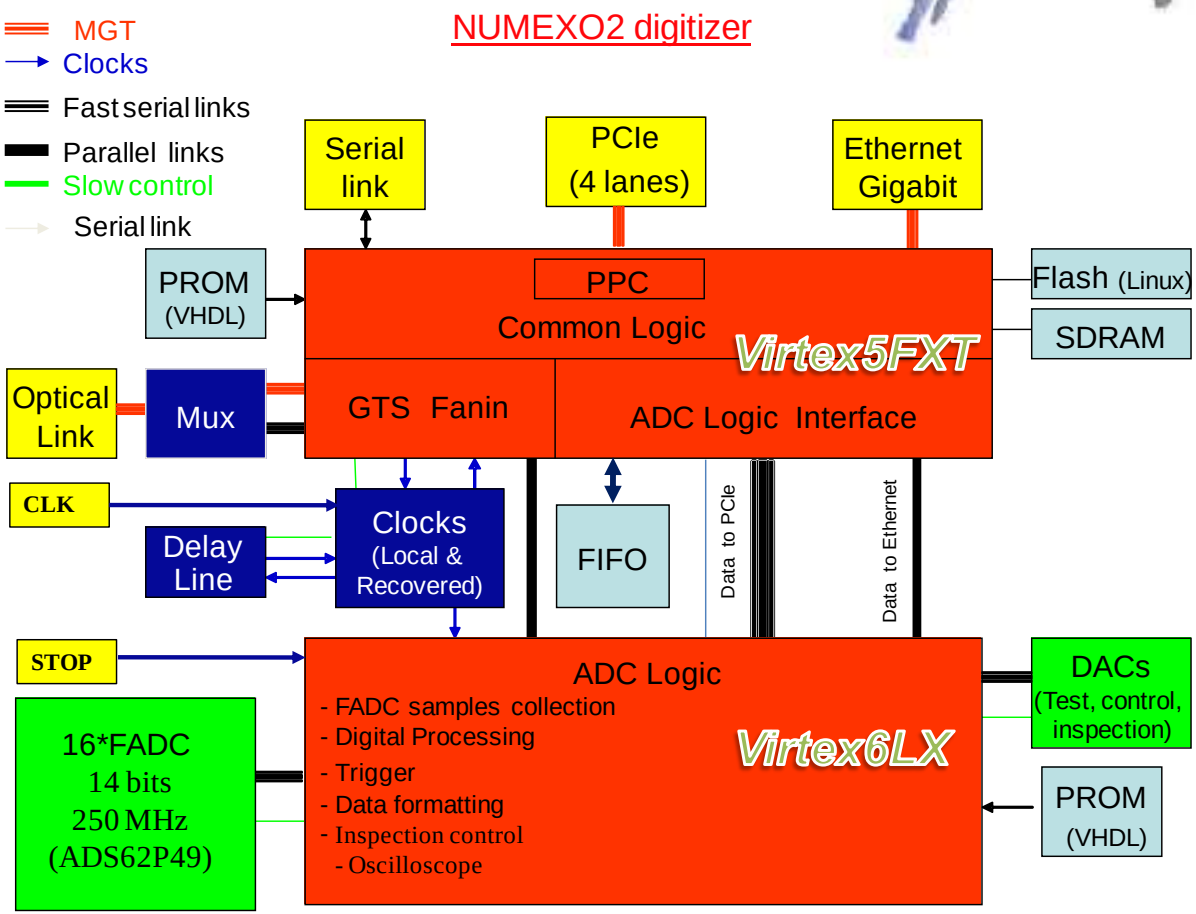


Digitizer

- Final specs early 2011 (synergy with NEDA, PARIS, S3)
- 16 channels NIM board
- Motherboard+ 4 FADC mezzanines

Overall status:

- All IPs identified and implemented in V5
- 45 sheets of schematics in CAD
- Schematics being cross-checked before final approval
- All critical components purchased



Virtex 5 (GANIL, Krakow, Warsaw, IPNO)

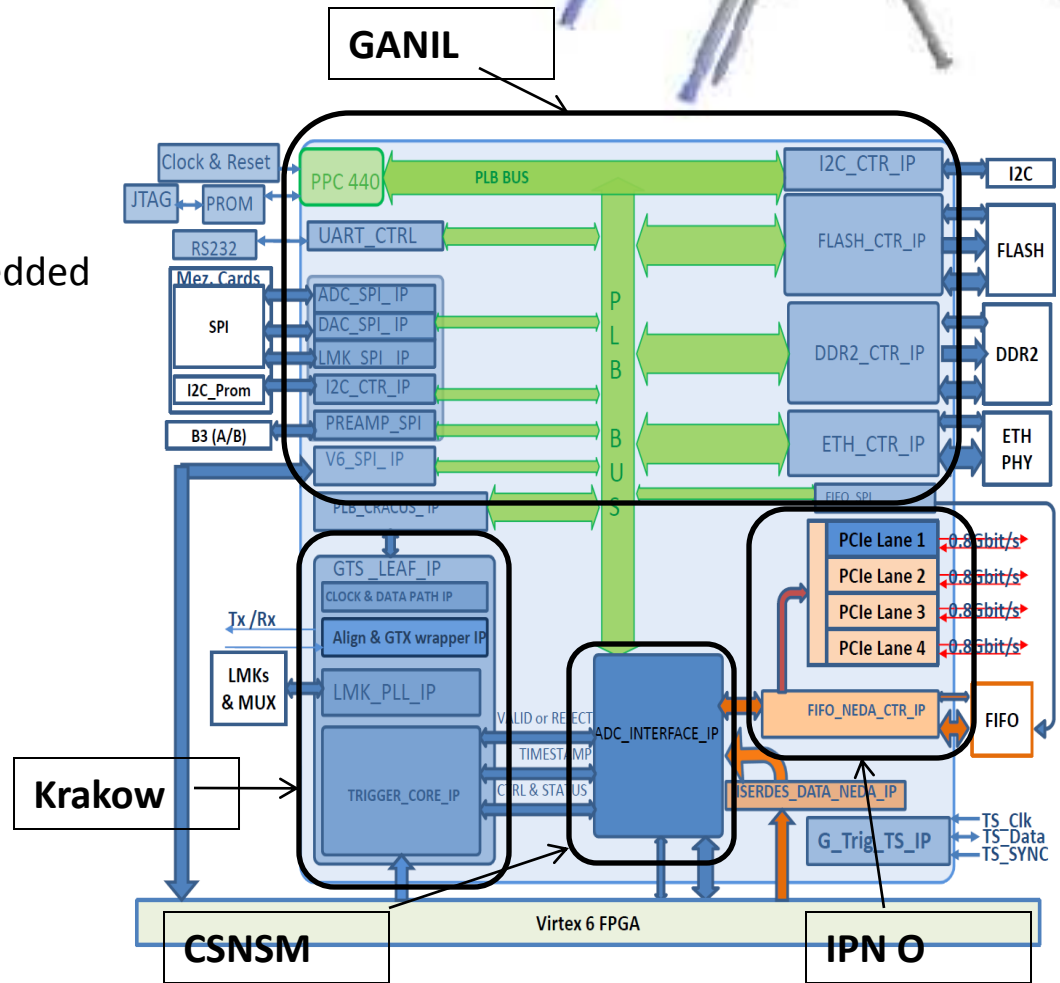
Role:

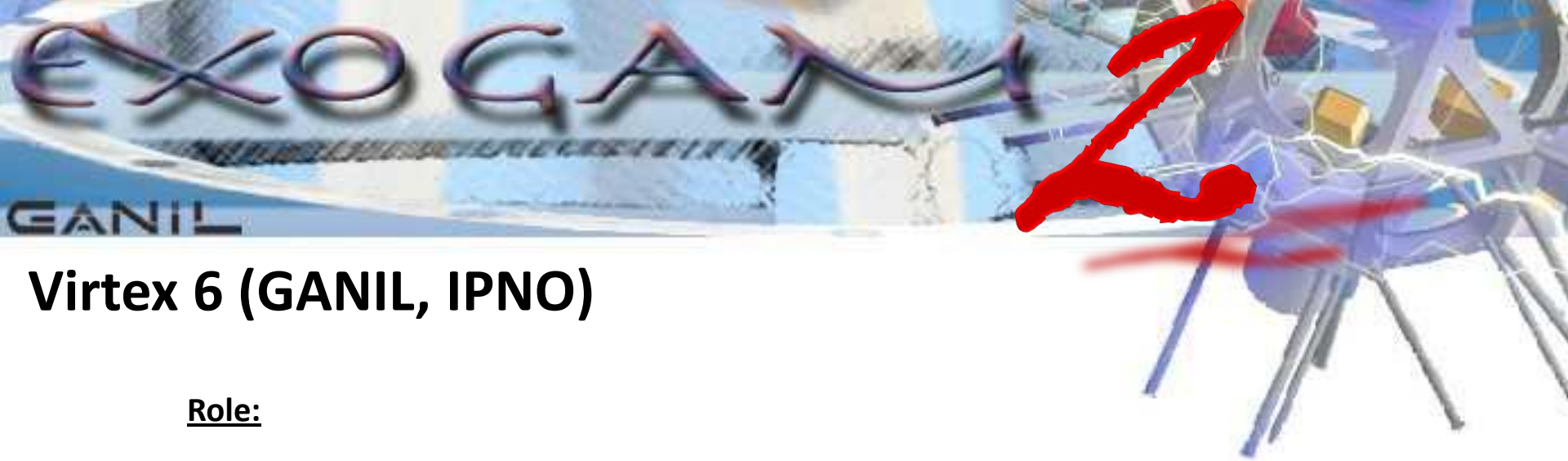
• V5: based on an FPGA integrated PowerPC(PPC405) associated to several Components (DDR2, FLASH…) to ensure Embedded Linux functionalities:

- ✓ Fast data readout (PCIexpress)
- ✓Global Triggering and time Stamping
- ✓Slow control

Status:

• All IPs identified and implemented in V5





Virtex 6 (GANIL, IPNO)

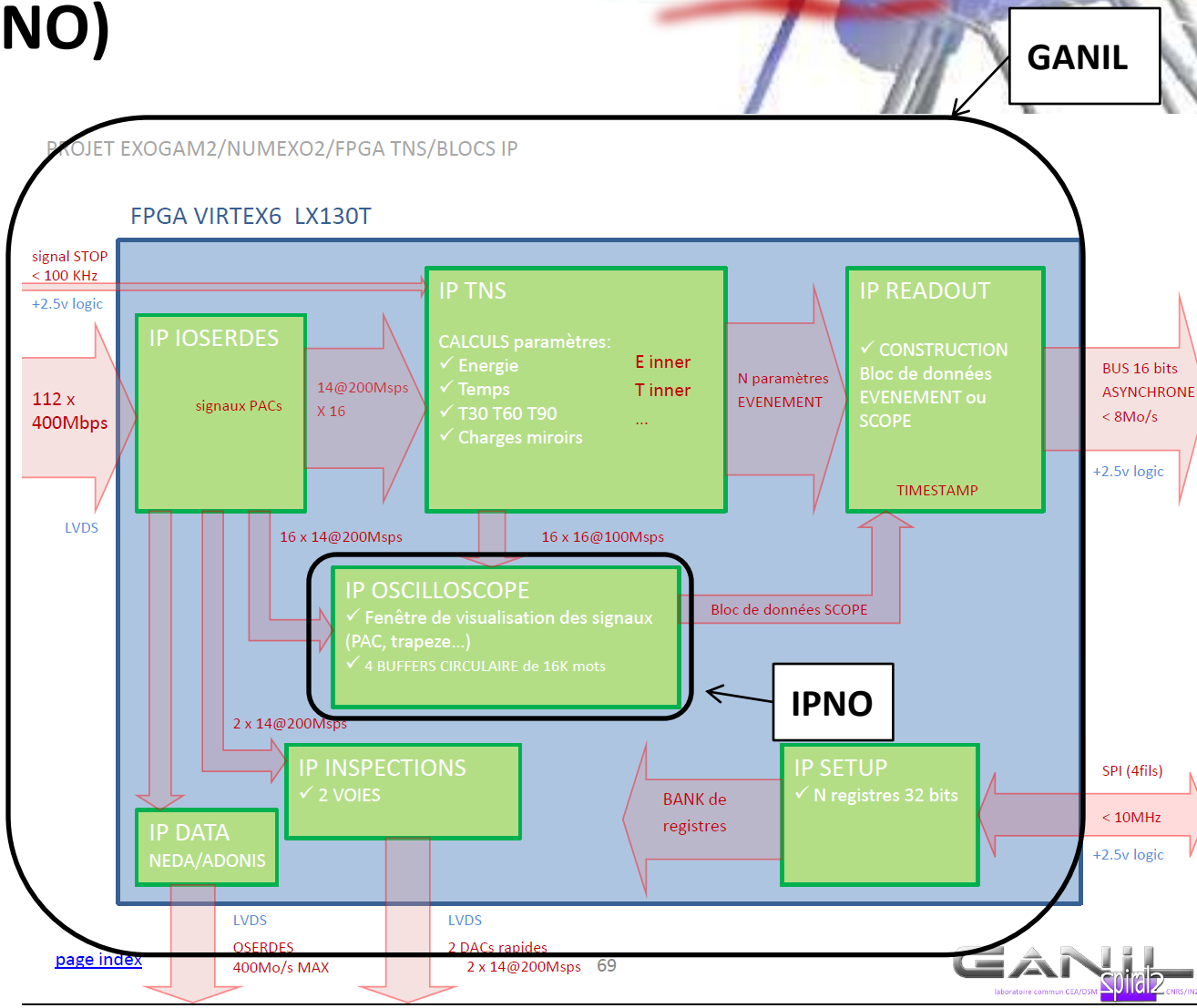
Role:

- Collects data from the 16 FADCs
- deals with data flow of 56Gbytes/s
- Measurement of:
  - ✓Energy
  - ✓Time
  - ✓Rise time (T30, T60, T90)
- Produce trigger signals for the two central contacts
- Tools for analysis, inspection, test and debugging
- Transmit deserialized and processed data to the V5 (parallel bus)
- Transmit raw data via a 400 MHz serial bus for NEDA and ADONIS (dedicated deported software to analyze data)

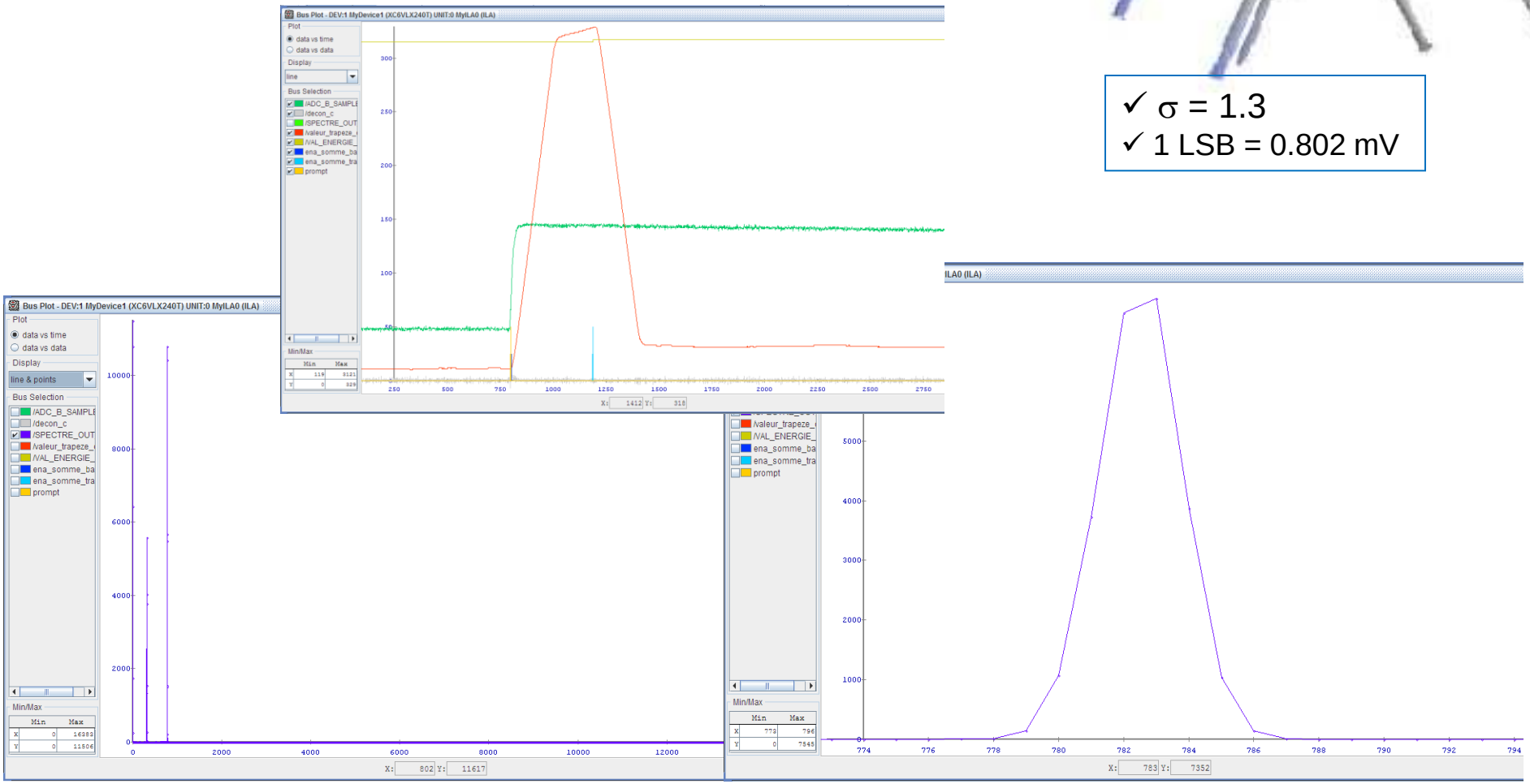
Virtex 6 (GANIL, IPNO)

Status:

- Firmware completed (except oscilloscopy)
- I/O assignment completed
- component choosen : VIRTEX6 LX130T
- Bank assignment underway



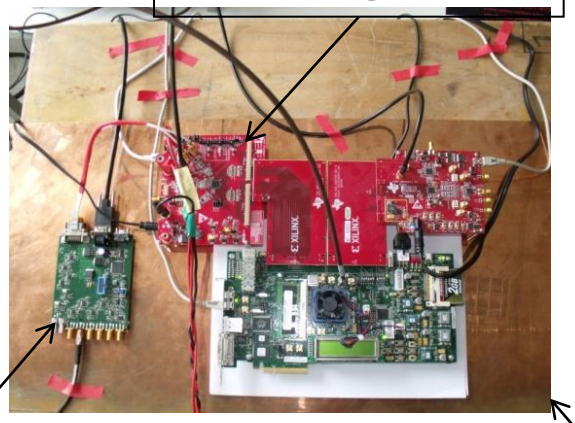
Embedded Logic Analyzer



- ✓ $\sigma = 1.3$
- ✓ 1 LSB = 0.802 mV

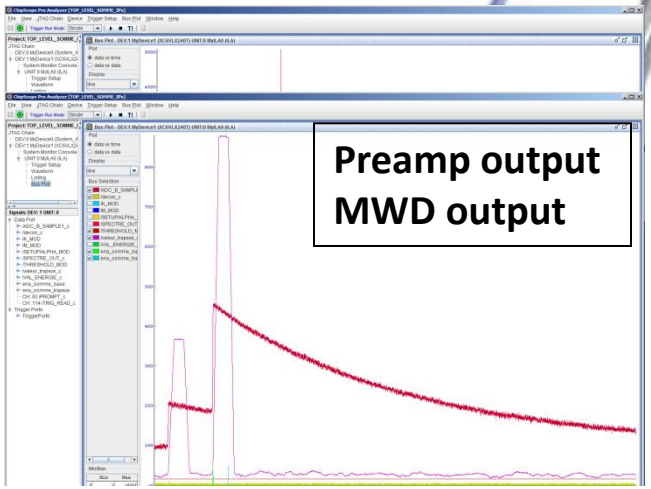
FADC 14 bits @ 250MHz + MWD: ^{60}Co spectrum

ADS62P49@250MHz

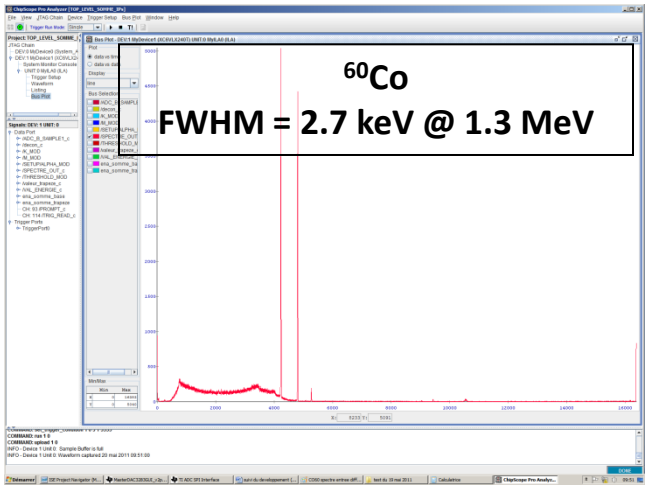


Connexion box

ML605



EXOGAM clover

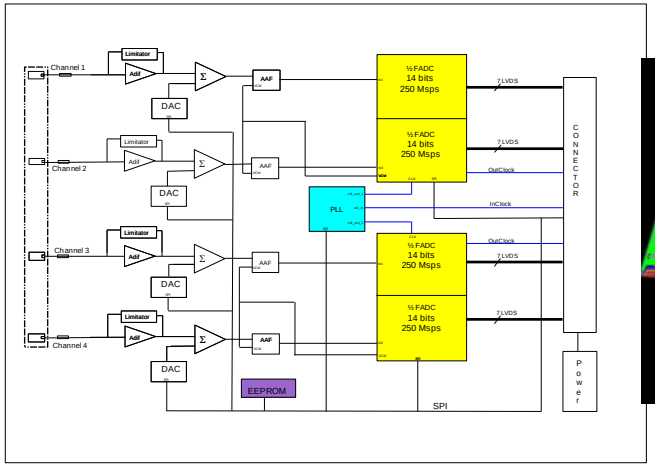


FADC Mezzanine (Valencia, GANIL)

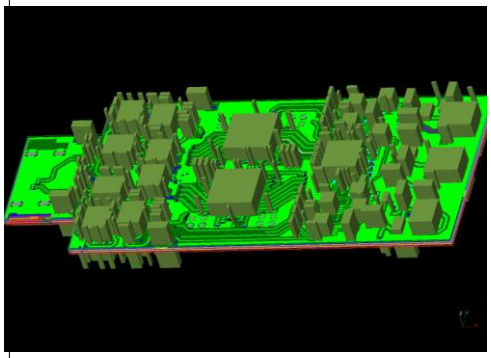
Spec:

- 4 analog differential inputs, 100Ω impedance
- analog bandwidth < 100MHz.
- FADC conversion: from 100MHz to 250MHz, 14 bits.
- sampling frequency controlled by a PLL: 100MHz input reference clock.
- adjustable gain stage for FADC amplitude range matching
- FADC common mode voltage control
- identification registers
- SPI control

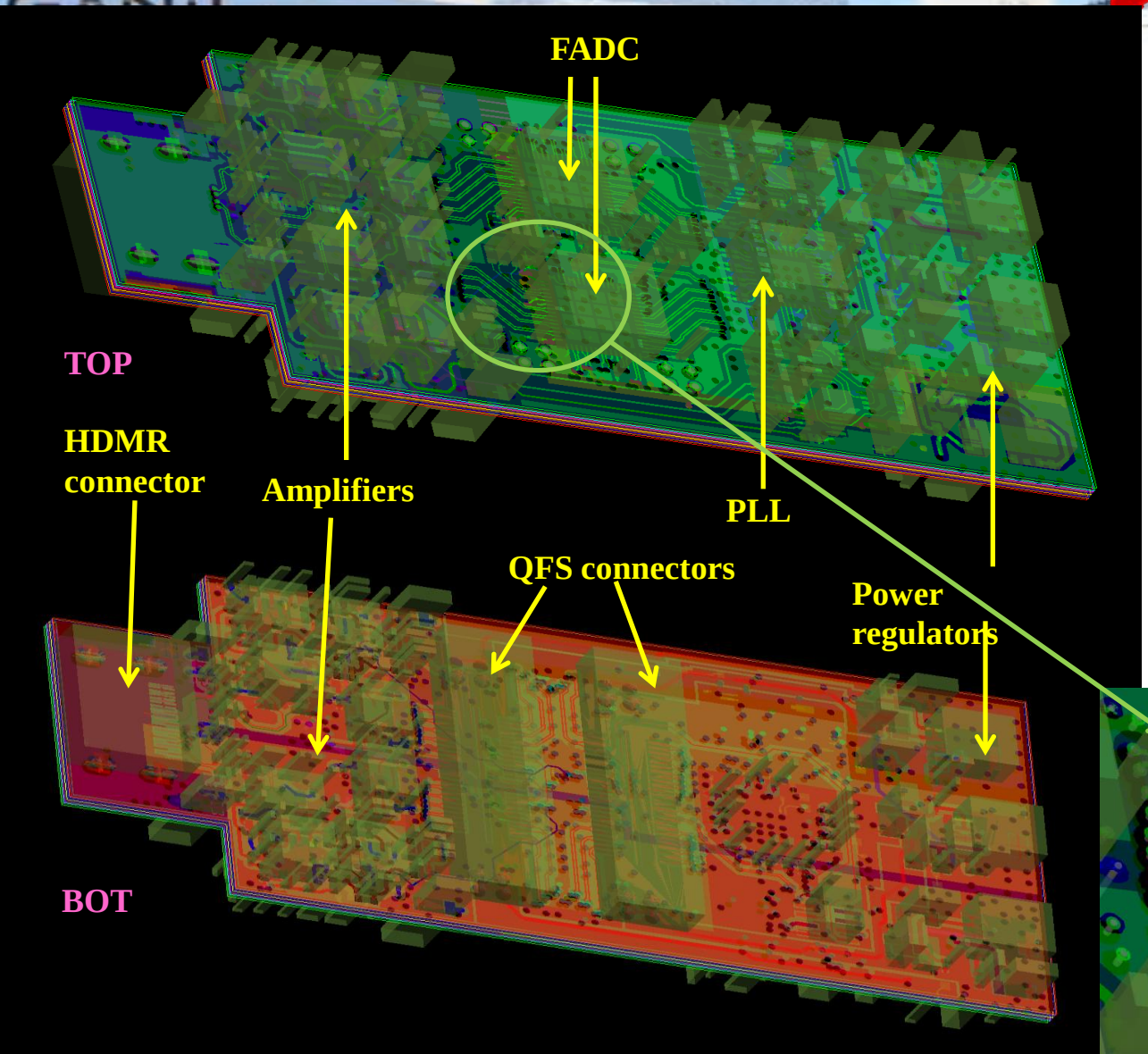
FADC Mezzanine Block Diagram 17 / 02 / 2011 Xavier Egea Canet



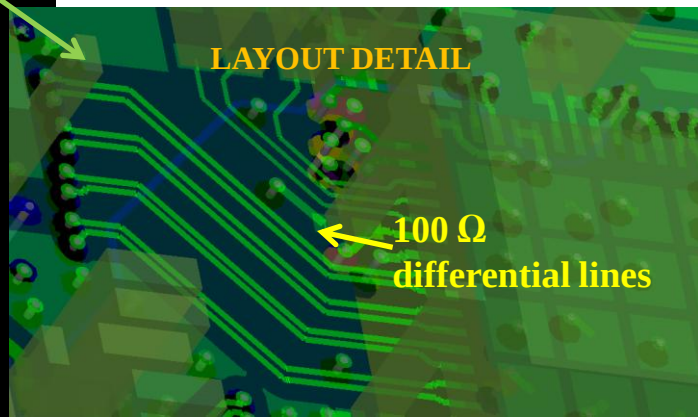
FADC mezzanine 3D top view



FADC Layout



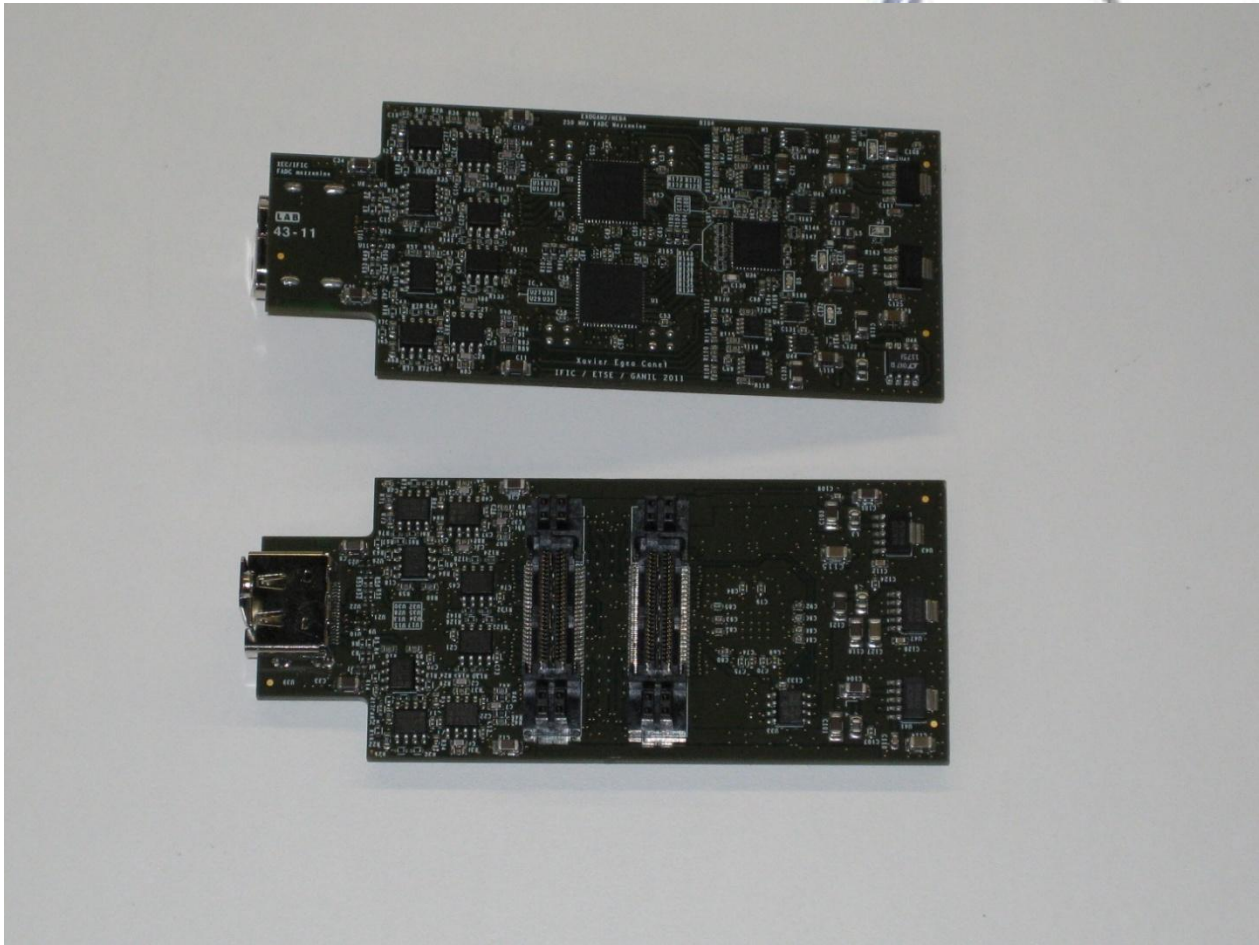
- 10 layers
- Straightforward way to place components
- Both connectors placed on the bottom layer



FADC Mezzanine status

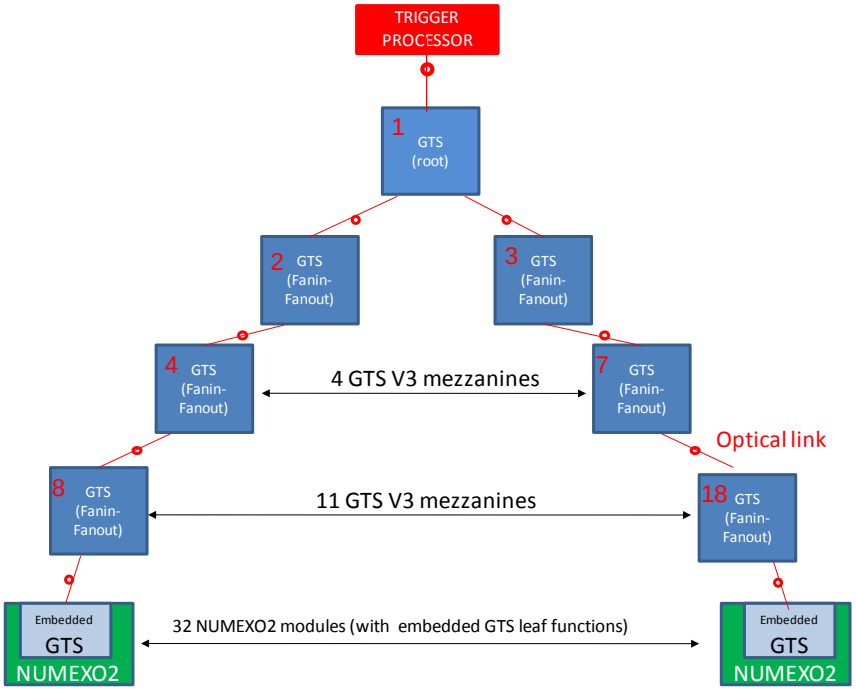
- Prototypes manufactured and under tests in Valencia

- Test bench designed and built



GTS (Krakow, GANIL, IUAC New Delhi)

- Developped for AGATA
  - ✓Clock distribution
  - ✓Time stamping
  - ✓Trigger decision
- Parts to be adapted to EXOGAM2:
  - ✓GTS leaf integration in the digitizer
  - ✓GTS carrier
- Need:
  - ✓32 GTS leaf functions embedded in digitizer
  - ✓18 GTS mezzanines (17 fan in/out; 1 root)
  - ✓1 trigger processor
- **Status:**
  - ✓GTS leaf design ready
  - ✓ IPs (firmware) under development
  - ✓ Carrier design completed
  - ✓Trigger processor: commercial cards bought



ADONIS (LIST,GANIL)

Status:

- ADONIS is compliant with signals coming from resistive preamplifiers (CSP). Measured resolution 2,3keV at 1.33MeV.
- Every gamma is time stamped
- There is no dead time ; no event is rejected
- The ‘separation’ analysis parameter sorts pulses regarding dead time and resolution.
- ADONIS processing is extremely efficient at high counting rate
- The ADONIS setup is independent of the counting rates. Filter parameters set up at low counting rate were kept for very high counting rate up to 120 kHz).
- Data transmission via PCIe (400 Mbytes/s)

To be done:

- Determine decimation level and extra parameters required for the correlation of events sourced from ADONIS system and Narval acquisition

Embedded software (GANIL)

Operating system

Linux as embedded operating system. It has been ported on the Virtex5 of the 2nd prototype (NUMEXO2_P2)

Register server

A register server has been developed to make the setup and the monitoring of the board. It acts as a client of the Electronics Control process.

Oscilloscope functionality

Send traces ViGRU (histogram display).

Data readout

To be done.

GTS

The GTS software running under VxWorks has to be ported under Linux, and adapted to the NUMEXO2_P2 context.

Software (GANIL)

- **Electronics control**

  A specific plug-in for the NUMEXO2_P2 has to be developed in the GANIL general Electronics Control framework

- **Histogram display**

  ViGru to display histograms. A specific client has been added to the application to get histograms directly from the embedded histogram server. FFT functionality has been implemented.

- **Data flow**

  The data readout will be made by using the Narval framework. An input actor in the Narval data flow has already been developed for test. An event builder actor is under development to merge the different branches of the system when several NUMEXO2 boards are used (32 boards for full EXOGAM2 configuration)

Collaborations/budget/planning

- Collaboration agreement active (more than 3 parties have signed)
- Collaborators:

GANIL, CNRS/IN2P3/CSNSM, KTH Stockholm*, ATOMKI Debrecen, Nigde Univ. , CNRS/IN2P3/IPNO, IFJ PAN Krakow, IUAC New Delhi, TIFR Mumbai.

Table B.2 Capital investment and human resources for EXOGAM2, and planned sharing between the participating collaborating parties. Spent (July 2011): 101 k€.

		Capital investment in k€ (2009-2013)	Personnel in person months (2009-2013)
Party	GANIL (including its contributions via FP7 SPIRAL2-PP and CPER[1])	372	130
	KTH	30[2]	-
	CSNSM	-	36
	IPNO	30	40
	IFJ PAN	30	40
	IUAC	-	6
	TIFR	100 (inc. Manpower)	6
	Nigde Univ.	61	-
	ATOMKI	45[3]	6
Other contributions	EXOGAM[4]	66	-
	Total	**579**	**264**

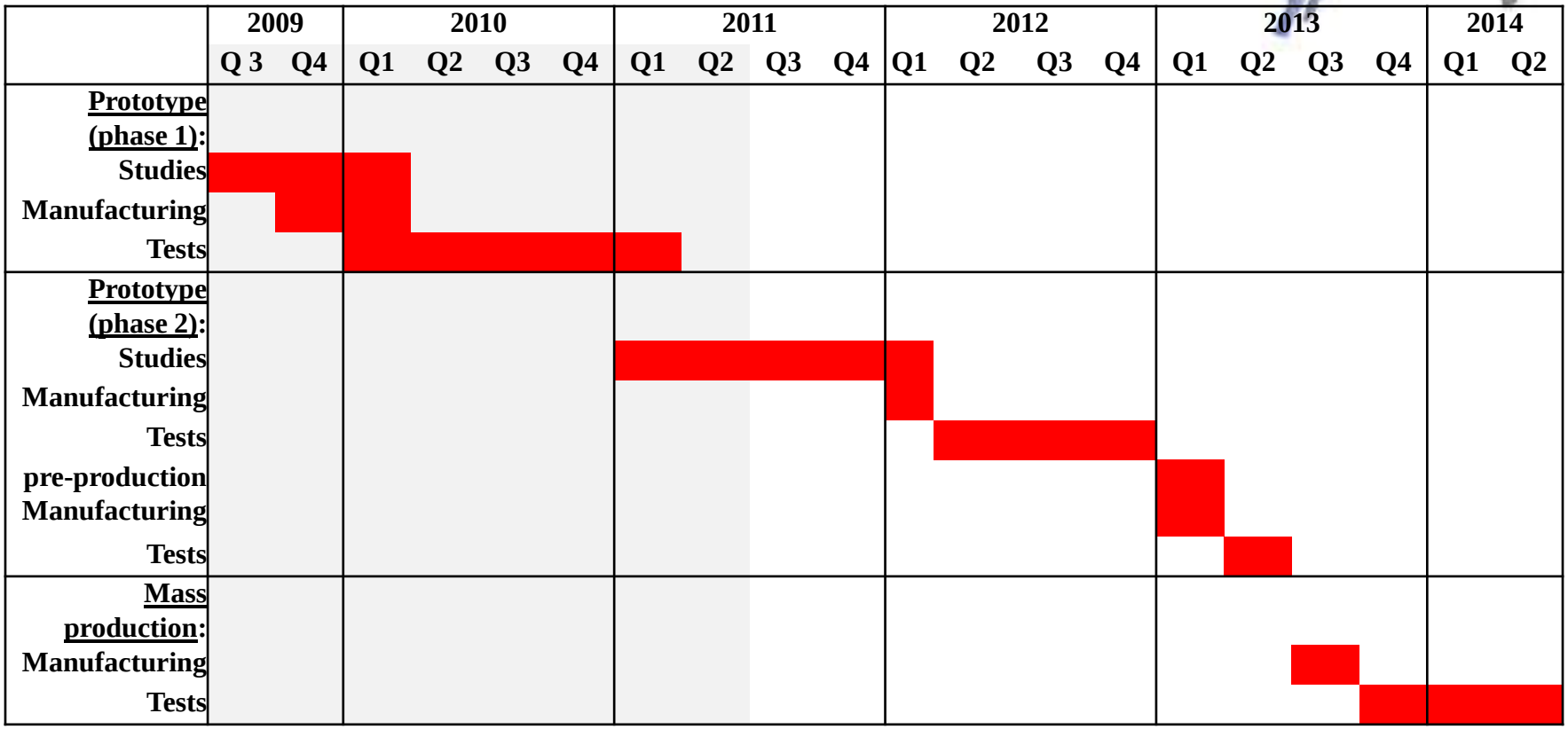
Planning d'investissement

Coût estimatif de l'électronique pour 16 clovers

	Quantité	Prix/unité (k€)	2011	2012	2013	Total (k€)
Interconnection box:						
Prototype	4	2	8			**8**
Serie	64+6	1		70		**70**
Cables:						
MDR 14 pin ou HDMI	128+12	0.1	1,2		12,8	**14**
Optical fibers and transceivers	32+4	1	4		32	**36**
FADC mezzanines						
FADC mezzanines prototypes	6	2	4	8		**12**
FADC mezzanines (serie)	128 + 12	1		140		**140**
Digitizer						
NIM 16 channels module (prototypes)	4	10	20	20		**40**
NIM 16 channels module (serie)	32+3	5			135	**135**
NIM crate	3	10	10		20	**30**
GTS tree:						
GTS NIM carrier (prototype)	1	2	2			**2**
GTS NIM carrier (serie)	5	2		10		**10**
GTS mezzanine	18+2	2.5	50			**50**
NIM crate	1	10		10		**10**
GTS supervisor	1+1	10		20		**20**
Switch 48 voies	1	2			2	**2**
TOTAL (k€)			99,2	278	201,8	**579**


EXOGAM
GANIL

Planning


2009
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Q4
Q1
Q2
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Q4
Q1
Q2
Q3
Q4
Q1
Q2
Prototype (phase 1):
Studies
Manufacturing
Tests
Prototype (phase 2):
Studies
Manufacturing
Tests
pre-production Manufacturing
Tests
Mass production:
Manufacturing
Tests

Conclusions

- Final specifications approved early 2011: synergy with NEDA (FADC, trigger requests, readout), PARIS, S3 ➔ flexibility, integration at GANIL, maintenance and support
- Tasks are progressing according planning
- Documentation written (detailed design spec., development roadmap, critical path analysis, collaboration agreement,…)
- Mass production to be clarified(TIFR/BARC?)
- Next major milestone: the full digitizer prototype (order in March and tests from May until end of 2012.